



Arm[®] Cortex[®]-A320 Core

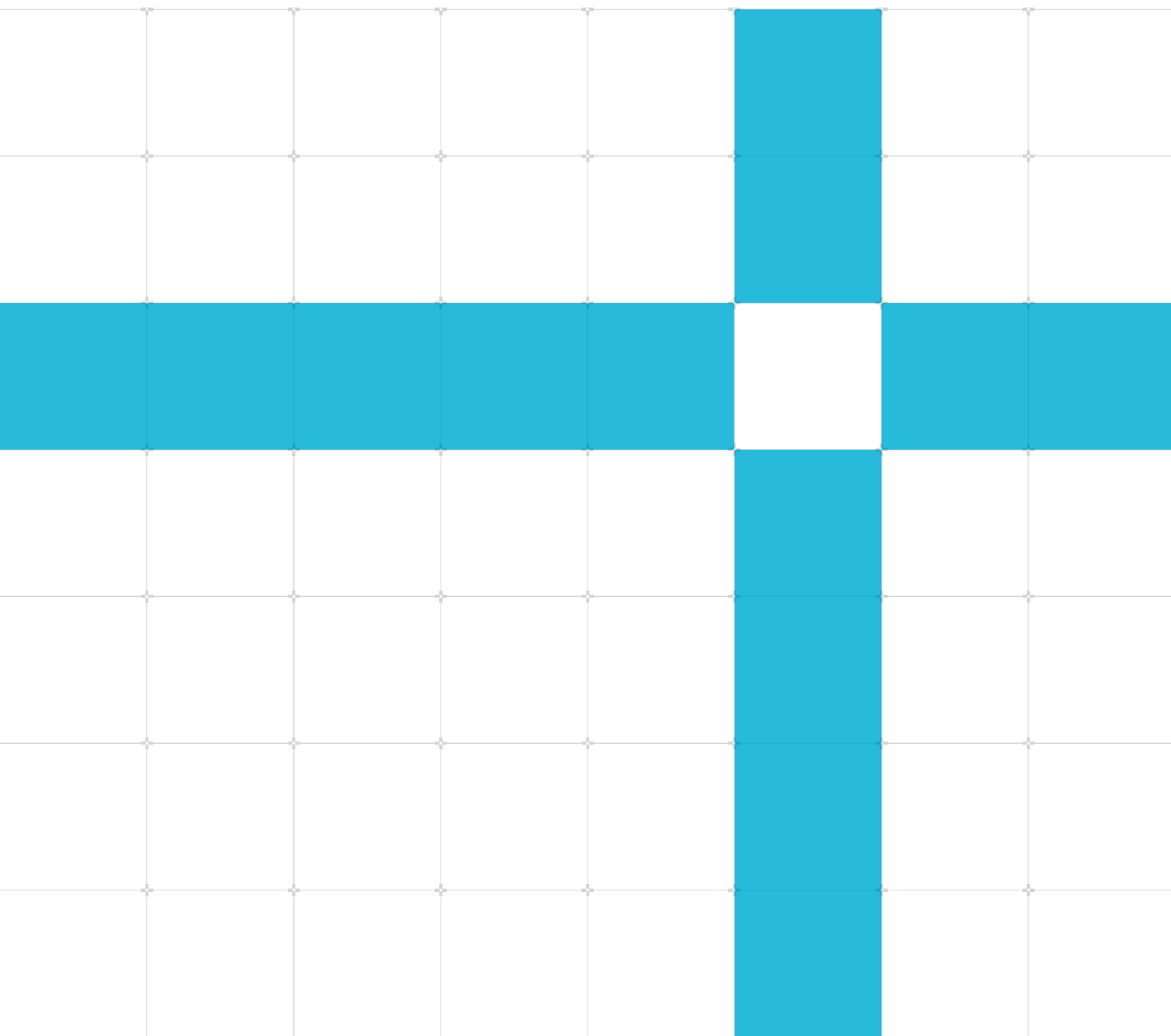
Software Optimization Guide

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Arm® Cortex®-A320 Core Software Optimization Guide

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See also: [Product and document information](#) | [Useful Resources](#)

Start reading

If you prefer, you can skip to [the start of the content](#).

Intended audience

This document is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses an Arm core.

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1 Introduction

1.1 Intended audience

This document is for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses an Arm core.

1.2 Conventions

The following subsections describe conventions used in Arm documents.

1.2.1 Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: <https://developer.arm.com/glossary>.






Terms and abbreviations


This document uses the following terms and abbreviations.

Convention	Use
ALU	Arithmetic and Logical Unit
ASIMD	Advanced Single Instruction Multiple Data
FP	Floating-point
GPR	General Purpose Register
SQRT	Square Root
SVE	Scalable Vector instruction Extension (SVE or SVE2)
VPR	Vector Processing Register; FP/ASIMD/SVE registers
VPU	Vector Processing Unit

1.2.2 Typographical conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
<i>italic</i>	Citations.
bold	Terms in descriptive lists, where appropriate.
monospace	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
<u>monospace underlined</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <code>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></code>
SMALL CAPITALS	Terms that have specific technical meanings as defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.
 Caution	We recommend the following. If you do not follow these recommendations your system might not work.
 Warning	Your system requires the following. If you do not follow these requirements your system will not work.
 Danger	You are at risk of causing permanent damage to your system or your equipment, or of harming yourself.
 Note	This information is important and needs your attention.
 Tip	This information might help you perform a task in an easier, better, or faster way.

Convention	Use
 Remember	This information reminds you of something important relating to the current content.

1.3 Useful resources

This document contains information that is specific to this product. See the following resources for other relevant information.

Access to Arm documents depends on their confidentiality:

- Arm Non-Confidential documents are available at <https://developer.arm.com/documentation>. Each document link in the tables below provides direct access to the online version of the document.
- Arm Confidential documents are available to licensees only through the product package.

Arm product resources	Document ID	Confidentiality
<i>Arm® Cortex®-A320 Core Technical Reference Manual</i>	109551	Non-Confidential
<i>Arm® Cortex®-A320 Core Configuration and Integration Manual</i>	109552	Confidential
<i>Arm® Cortex®-A320 Core Cryptographic Extension Technical Reference Manual</i>	109553	Non-Confidential
<i>Arm® Cortex®-A320 Core Release Note</i>	-	Non-Confidential
<i>Arm® DynamIQ™ Shared Unit 120 (DSU-120) Technical Reference Manual</i>	102547	Non-Confidential
<i>Arm® DynamIQ™ Shared Unit 120 (DSU-120) Configuration and Integration Manual</i>	102548	Confidential

Arm architecture and specifications	Document ID	Confidentiality
<i>Arm® Architecture Reference Manual for A-profile architecture profile</i>	DDI 0487	Non-Confidential
<i>Arm® CoreSight™ Architecture Specification v3.0</i>	IHI 0029	Non-Confidential
<i>Arm® CoreSight™ ELA-600 Embedded Logic Analyzer Configuration and Integration Manual</i>	101089	Confidential
<i>Arm® CoreSight™ ELA-600 Embedded Logic Analyzer Technical Reference Manual</i>	101088	Non-Confidential
<i>Arm® Generic Interrupt Controller Architecture Specification, GIC architecture version 3 and version 4</i>	IHI 0069	Non-Confidential

Arm architecture and specifications	Document ID	Confidentiality
<i>Arm® Memory System Resources Partitioning and Monitoring (MPAM) System Component Specification</i>	IHI 0099	Non-Confidential
<i>AMBA® AXI Protocol Specification</i>	IHI 0022	Non-Confidential

Non-Arm resources	Document ID	Organization
<i>IEEE, Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device</i>	1687-2014	IEEE
<i>IEEE, Standard for Design and Verification of Low-Power, Energy-Aware Electronic Systems</i>	1801-2009	IEEE

2 Product Overview

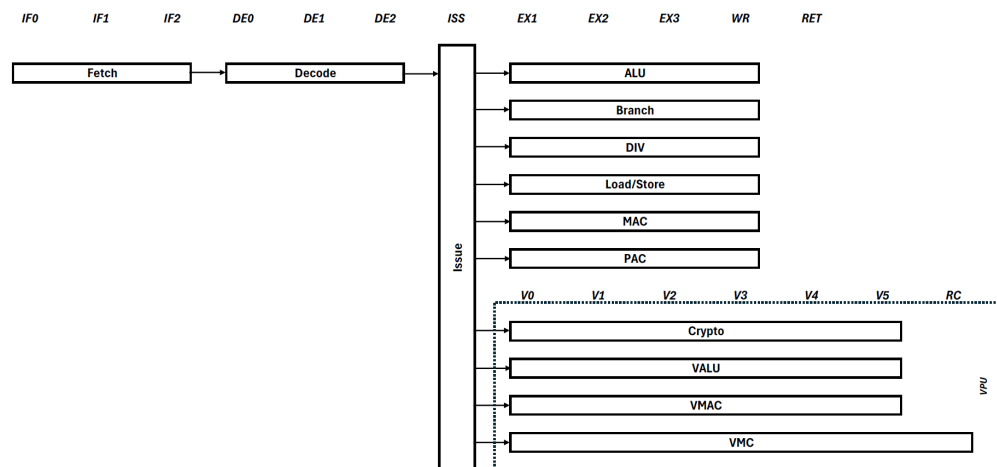
Cortex®-A320 Core is a ultra-efficiency, low-power product that implements the Arm® v9.2-A architecture. The Arm® v9.2-A architecture extends the architecture defined in the Arm® v8-A architectures up to Arm® v8.7-A. The key features of Cortex®-A320 Core are:

- Implementation of the Arm® v9.2-A A64 instruction set.
- AArch64 Execution state at all Exception levels, EL0 to EL3.
- Separate L1 data and instruction side memory systems with a Memory Management Unit (MMU).
- In-order pipeline with direct and indirect branch prediction.
- Generic Interrupt Controller (GIC) CPU interface to connect to an external interrupt distributor.
- Generic Timer interface that supports a 64-bit count input from an external system counter.
- Implementation of the Reliability, Availability, and Serviceability (RAS) Extension.
- 128-bit Scalable Vector Extension (SVE) and SVE2 SIMD instruction set, offering Advanced SIMD (ASIMD) and floating-point (FP) architecture support.
- Support for the optional Cryptographic Extension, which is licensed separately.
- Activity Monitoring Unit (AMU).
- Quad/Dual/Single Core configuration option: All cores in the complex share the L2 cache. The VPU is shared by up to two cores. In quad-core configurations two VPUs will be present. Single-core complexes have a dedicated L2 cache and VPU. Figure 2-1 highlights the VPU pipelines shared between Cortex®-A320 cores in a complex.
- The vector datapath includes two 64-bit pipelines. Figure 2-1 highlights the VPU pipelines that instantiated for a 2x64-bit configuration.

This document describes the elements of Cortex®-A320 Core micro-architecture that influence the software performance so that software and compilers can be optimized accordingly.

2.1 Pipeline overview

Figure 2-1: Cortex®-A320 Core pipeline.



The execution pipelines support different types of operations, as shown in the following table.

Table 2-1: Cortex®-A320 Core Pipeline

Pipeline	Instructions
ALU	Arithmetic and logic
Branch	Branch
Crypto	Cryptography Supports 1x128-bit operation. This pipeline is shared for multiple core configuration. Present only for implementations configured with Cryptographic. Extensions enabled.
DIV	Integer scalar division (iterative)
Load/Store	Load and store
MAC	Multiply accumulate
PAC	Pointer Authentication
VALU	Addition, logic and shift for ASIMD, FP, Neon, and SVE Supports 2x64-bit. This pipeline is shared for multiple core configuration.
VMAC	Multiply accumulate for ASIMD, FP, Neon, and SVE Supports 2x64-bit or 1x128-bit operations.

Pipeline	Instructions
	This pipeline is shared for multiple core configurations.
VMC	Cryptography and iterative multi cycle instruction (e.g. bit permutation, division, and square root) Supports 2x64-bit operations. This pipeline is shared for multiple core configurations.

3 Instruction characteristics

3.1 Instruction tables

This chapter describes high-level performance characteristics for most Arm® v9-A instructions. A series of tables summarize the effective execution latency and throughput (instruction bandwidth per cycle), pipelines utilized, and special behaviors associated with each group of instructions. Utilized pipelines correspond to the execution pipelines described in subsection 2.1. In the tables below:

- *Execution Latency* is the minimum latency seen by an operation dependent on an instruction in the described group.
- *Load Latency* is the minimum latency seen by an operation dependent on the load. It is assumed the memory access hits in the L1 Data Cache.
- *Execution Throughput* is maximum throughput (in instructions per cycle) of the specified instruction group that can be achieved in the entirety of Cortex®-A320 Core microarchitecture.

3.2 Branch Instructions

Table 3-1: AArch64 Branch instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Branch, immed	B	-	1	Branch
Branch, register	BR, RET	-	1	Branch
Branch and link, immed	BL	1	1	Branch
Branch and link, register	BLR	1	1	Branch
Compare and branch	CBZ, CBNZ, TBZ, TBNZ	-	1	Branch

3.3 Arithmetic and logical instructions

Table 3-2: AArch64 Arithmetic and logical instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Arithmetic, basic	ADD, ADC, SBC, SUB, NEG	1	1	ALU
Arithmetic, basic, flagset	ADDS, SUBS	1	1	ALU
Arithmetic, basic, carry, flagset	ADCS, SBCS	1	1	ALU
Arithmetic, extend and shift	ADD, ADDS, SUB, SUBS, NEG	2 ^[1]	1	ALU
Compare	CMN, CMP	1	1	ALU
Conditional compare	CCMN, CCMP	1	1	ALU
Conditional select	CSEL, CSINC, CSINV, CSNEG	1	1	ALU
Logical, basic	AND, ANDS, BIC, BICS, EON, EOR, ORN, ORR	1	1	ALU
Logical, shift	AND, ANDS, BIC, BICS, EON, EOR, ORN, ORR	1	1	ALU

3.4 Divide and multiply instructions

Integer divides are performed using an iterative algorithm and block any subsequent divide operations until complete. Early termination is possible, depending upon the data values.

Table 3-3: AArch64 Divide and multiply instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Divide, W-form	SDIV, UDIV	12	1/12	DIV
Divide, X-form	SDIV, UDIV	20	1/20	DIV

^[1] Latency=2 when the dependency is on Rm.

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Multiply accumulate, W-form	MADD, MSUB, MUL	3	1	MAC
Multiply accumulate, X-form	MADD, MSUB, MUL	4	1/2	MAC
Multiply accumulate long	SMADDL, SMSUBL, UMADDL, UMSUBL	2	1	MAC
Multiply high	SMULH, UMULH	6	1/4	MAC

3.5 Pointer authentication instructions

Table 3-4: AArch64 Pointer authentication instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Authenticate data address	AUTDA, AUTDB, AUTDZA, AUTDZB	4	1	PAC
Authenticate instruction address	AUTIA, AUTIB, AUTIA1716, AUTIB1716, AUTIASP, AUTIBSP, AUTIAZ, AUTIBZ, AUTIZA, AUTIZB	4	1	PAC
Branch and link, register, with pointer authentication	BLRAA, BLRAAZ, BLRAB, BLRABZ	1	1	Branch, PAC
Branch, register, with pointer authentication	BRAA, BRAAZ, BRAB, BRABZ	-	1	Branch, PAC
Branch, return, with pointer authentication	RETA, RETB	-	1	Branch
Compute pointer authentication code for data address	PACDA, PACDB, PACDZA, PACDZB	4	1	PAC
Compute pointer authentication code, using generic key	PACGA	5	1	PAC

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Compute pointer authentication code for instruction address	PACIA, PACIB, PACIA1716, PACIB1716, PACIASP, PACIBSP, PACIAZ, PACIBZ, PACIZA, PACIZB	4	1	PAC
Load register, with pointer authentication, offset	LDRAA, LDRAB	4	1	PAC
Load register, with pointer authentication, pre-indexed	LDRAA, LDRAB	4	1	PAC
Strip pointer authentication code	XPACD, XPACI, XPACLRI	4	1	PAC

**Note**

1. There is a dedicated forwarding path in the accumulate portion of the unit that allows the result of one MAC operation to be used as the accumulate operand of a following MAC operation with no interlock. Thanks to this, a typical sequence of multiply-accumulate instructions can issue one every 2 cycles). Accumulator forwarding is not supported for consumers of 64 bit multiply high operations.
2. Latency and throughput numbers given for SDIV and UDIV are the worst-case values. Early termination is possible, depending upon the data values (for example, degenerate cases such as divide by zero). Integer divides are performed using an iterative algorithm and block any subsequent divide operations until complete. The number of cycles needed to execute these instructions can be calculated using the formula $[N + \text{bits}/4]$ ($N=3$ for UDIV, $N=4$ for SDIV, i.e. signed division takes one more cycle than unsigned division).

3.6 Miscellaneous data processing instructions

Table 3-5: AArch64 miscellaneous data processing instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Address generation	ADR, ADRP	1	1	ALU
Bitfield extract	EXTR	2 ^[2]	1	ALU
Bitfield move, basic	SBFM, SBFIZ, SBFX, SXTB, SXTW, UBFM, UBFIZ, UBFX, UXTH	2 ^[3]	1	ALU
Bitfield move, insert	BFC, BFI, BFM	2	1	ALU
Convert floating-point condition flags	AXFLAG, XAFLAG	-	1	ALU
Flag set instructions	SETF8, SETF16	2	1/2	ALU
Flag manipulation instructions, rotate and select	RMIF	1	1	ALU
Flag manipulation instructions, invert carry	CFINV	1	1	ALU
Count leading	CLS, CLZ	1	1	ALU
Move	MOV, MOVN, MVN, MOVK, MOVZ	1	1	ALU
Reverse bytes	REV, REV16, REV32	1	1	ALU
Reverse bits	RBIT	2	1	ALU
Variable shift	ASR, ASRV, LSL, LSLV, LSR, LSRV, ROR, RORV	1	1	ALU
Extend, sign or zero	SXTB, UXTB	1	1	ALU

^[2] Latency=1 for ROR (immediate) alias of EXTR.

^[3] Latency=1 for LSL (immediate), LSR (immediate) and UXTB aliases of UBFM. Latency=1 for SXTB and ASR (immediate) aliases of SBFM.

3.7 Load instructions

The latencies shown in Table 3-6 assume the memory access hits in the Level 1 Data Cache. Base register updates are done in parallel to the operation.

Table 3-6: AArch64 Load instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Load register, literal	LDR, LDRSW, PRFM	4	1	Load/Store
Load register, unscaled immediate	LDUR, LDURB, LDURH, LDURSB, LDURSH, LDURSW, PRFUM	4	1	Load/Store
Load register, immediate post-index	LDR, LDRB, LDRH, LDRSB, LDRSH, LDRSW	4	1	Load/Store
Load register, immediate pre-index	LDR, LDRB, LDRH, LDRSB, LDRSH, LDRSW	4	1	Load/Store
Load register, immediate unprivileged	LDTR, LDTRB, LDTRH, LDTRSB, LDTRSH, LDTRSW	4	1	Load/Store
Load register, unsigned immediate	LDR, LDRB, LDRH, LDRSB, LDRSH, LDRSW, PRFM	4	1	Load/Store
Load register, register offset, basic	LDR, LDRB, LDRH, LDRSB, LDRSH, LDRSW, PRFM	4	1	Load/Store
Load register, register offset, scale	LDR, LDRB, LDRSB, LDRSW, PRFM	4	1	Load/Store
Load register, register offset, scale, halfword	LDRH, LDRSH	4	1	Load/Store
Load register, register offset, extend	LDR, LDRB, LDRH, LDRSB, LDRSH, LDRSW, PRFM	4	1	Load/Store
Load register, register offset, extend, scaled	LDR, LDRB, LDRSW, LDRSB, PRFM	4	1	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Load register, register offset, extend, scaled, halfword	LDRH, LDRSH	4	1	Load/Store
Load pair, signed immediate offset, normal, W-form	LDP, LDNP	4	1	Load/Store
Load pair, signed immediate offset, normal, X-form	LDP, LDNP	4	1	Load/Store
Load pair, signed immediate offset, signed words	LDPSW	4	1	Load/Store
Load pair, immediate post-index or immediate pre-index, normal, W-form	LDP	4	1	Load/Store
Load pair, immediate post-index or immediate pre-index, normal, X-form	LDP	4	1	Load/Store
Load pair, immediate post-index or immediate pre-index, signed words	LDPSW	4	1	Load/Store

3.8 Store instructions

Base register updates are done in parallel to the operation.

Table 3-7: AArch64 Store instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store register, unscaled immediate	STUR, STURB, STURH	-	1	Load/Store
Store register, immediate post-index	STR, STRB, STRH	-	1	Load/Store
Store register, immediate pre-index	STR, STRB, STRH	-	1	Load/Store
Store register, immediate unprivileged	STTR, STTRB, STTRH	-	1	Load/Store
Store register, unsigned immediate	STR, STRB, STRH	-	1	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store register, register offset, basic	STR, STRB, STRH	-	1	Load/Store
Store register, register offset, scaled	STR, STRB	-	1	Load/Store
Store register, register offset, scaled, halfword	STRH	-	1	Load/Store
Store register, register offset, extend	STR, STRB, STRH	-	1	Load/Store
Store register, register offset, extend, scaled	STR, STRB	-	1	Load/Store
Store register, register offset, extend, scaled, halfword	STRH	-	1	Load/Store
Store pair, immediate offset	STP, STNP	-	1	Load/Store
Store pair, immediate post-index	STP	-	1	Load/Store
Store pair, immediate pre-index	STP	-	1	Load/Store

3.9 Tag data processing

Table 3-8: AArch64 Tag data processing instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Arithmetic, immediate to logical address tag	ADDG, SUBG	2	1	ALU
Insert Random Tags	IRG	4	1/3	ALU
Insert Tag Mask	GMI	2	1	ALU
Subtract Pointer	SUBP	2	1	ALU
Subtract Pointer, flagset	SUBPS	2	1	ALU

3.10 Tag load instructions

The latencies shown assume the memory access hits in the Level 1 Data Cache.

Table 3-9: Tag load instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Load allocation tag	LDG	4	1	Load/Store
Load multiple allocation tags	LDGM	7	1/4	Load/Store

3.11 Tag store instructions

Base register updates are done in parallel to the operation.

Table 3-10: AArch64 Tag store instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store allocation tags to one granule, post-index	STG	-	1	Load/Store
Store allocation tags to two granules, post-index	ST2G	-	1/2	Load/Store
Store allocation tags to one granule, pre-index	STG	-	1	Load/Store
Store allocation tags to two granules, pre-index	ST2G	-	1/2	Load/Store
Store allocation tags to one granule, signed offset	STG	-	1	Load/Store
Store allocation tags to two granules, signed offset	ST2G	-	1/2	Load/Store
Store allocation tag to one granule, zeroing, post-index	STZG	-	1	Load/Store
Store allocation tag to two granules, zeroing, post-index	STZ2G	-	1/2	Load/Store
Store Allocation Tag to one granule, zeroing, pre-index	STZG	-	1	Load/Store
Store Allocation Tag to two granules, zeroing, pre-index	STZ2G	-	1/2	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store allocation tag to one granule, zeroing, signed offset	STZG	-	1	Load/Store
Store allocation tag to two granules, zeroing, signed offset	STZ2G	-	1/2	Load/Store
Store allocation tag and reg pair to memory, post-Index	STGP	-	1	Load/Store
Store allocation tag and reg pair to memory, pre-Index	STGP	-	1	Load/Store
Store allocation tag and reg pair to memory, signed offset	STGP	-	1	Load/Store
Store multiple allocation tags	STGM	-	1	Load/Store
Store multiple allocation tags, zeroing	STZGM	-	1	Load/Store

3.12 Floating-point scalar data processing instructions

Table 3-11: AArch64 Floating-point scalar data processing instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
FP absolute value	FABS, FABD	4	1	VALU
FP arithmetic	FADD, FSUB, FADDP	4	1	VALU
FP conditional compare	FCCMP, FCCMPE	5	1/5	VALU
FP compare	FCMP, FCMPE	1	1	VALU
FP divide, H-form	FDIV	8	2/5	VMC
FP divide, S-form	FDIV	13	2/10	VMC
FP divide, D-form	FDIV	22	2/19	VMC
FP min/max	FMIN, FMINNM, FMAX, FMAXNM	4	1	VALU
FP max/min, pairwise	FMAXP, FMAXNMP, FMINP, FMINNMP	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
FP multiply	FMUL, FNMUL, FMULX	4	1	VMAC
FP multiply accumulate	FMADD, FMSUB, FNMADD, FNMSUB	4	1	VMAC
FP negate	FNEG	4	1	VALU
FP round to integral	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ, FRINT32X, FRINT64X, FRINT32Z, FRINT64Z	4	1	VALU
FP select	FCSEL	3	1	VALU
FP square root, H-form	FSQRT	11	2/5	VMC
FP square root, S-form	FSQRT	14	2/9	VMC
FP square root, D-form	FSQRT	25	2/19	VMC



Note

Floating-point division operations may finish early if the divisor is a power of two (normal with a zero trailing significand).

3.13 Floating-point scalar miscellaneous instructions

Table 3-12: AArch64 Floating-point scalar miscellaneous instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
FP convert, from gen to vec reg	SCVTF, UCVTF	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
FP convert, from vec to gen reg	FCVTAS, FCVTAU, FCVTMS, FCVTMU, FCVTNS, FCVTNU, FCVTPS, FCVTPU, FCVTZS, FCVTZU	4	1	VALU
FP convert, Javascript from vec to gen reg	FJCVTZS	4	1	VALU
FP convert, from vec to vec reg	FCVT, FCVTXN	4	1	VALU
FP move, immediate	FMOV	-	1	VALU
FP move, register	FMOV	3	1	VALU
FP transfer, from gen to vec reg	FMOV	-	1	VALU
FP transfer, from vec to gen reg	FMOV	-	1	VALU

3.14 Floating-point scalar load instructions

The latencies shown assume the memory access hits in the Level 1 Data Cache. Base register updates are done in parallel to the operation.

Table 3-13: AArch64 Floating-point scalar load instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Load vector reg, literal	LDR	3	1	Load/Store
Load vector reg, unscaled immediate	LDUR	3	1	Load/Store
Load vector reg, immediate post-index	LDR	3	1	Load/Store
Load vector reg, immediate pre-index	LDR	3	1	Load/Store
Load vector reg, unsigned immediate	LDR	3	1	Load/Store
Load vector reg, register offset, basic	LDR	3	1	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Load vector reg, register offset, scale	LDR	3	1	Load/Store
Load vector reg, register offset, extend	LDR	3	1	Load/Store
Load vector reg, register offset, extend, scale	LDR	3	1	Load/Store
Load vector pair, immediate offset, S/D-form	LDP, LDNP	3	1	Load/Store
Load vector pair, immediate offset, Q-form	LDP, LDNP	3	1/2	Load/Store
Load vector pair, immediate post-index, S/D-form	LDP	3	1	Load/Store
Load vector pair, immediate post-index, Q-form	LDP	3	1/2	Load/Store
Load vector pair, immediate pre-index, S/D-form	LDP	3	1	Load/Store
Load vector pair, immediate pre-index, Q-form	LDP	3	1/2	Load/Store

3.15 Floating-point scalar store instructions

Base register updates are done in parallel to the operation.

Table 3-14: AArch64 Floating-point scalar Store instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store vector reg, unscaled immediate	STUR	-	1	Load/Store
Store vector reg, immediate post-index	STR	-	1	Load/Store
Store vector reg, immediate pre-index	STR	-	1	Load/Store
Store vector reg, unsigned immediate	STR	-	1	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store vector reg, register offset, basic	STR	-	1	Load/Store
Store vector reg, register offset, scale	STR	-	1	Load/Store
Store vector reg, register offset, extend	STR	-	1	Load/Store
Store vector reg, register offset, extend	STR	-	1	Load/Store
Store vector pair, immediate offset, S-form	STP, STNP	-	1	Load/Store
Store vector pair, immediate offset, D-form	STP, STNP	-	1	Load/Store
Store vector pair, immediate offset, Q-form	STP, STNP	-	1/2	Load/Store
Store vector pair, immediate post-index, S-form	STP	-	1	Load/Store
Store vector pair, immediate post-index, D-form	STP	-	1	Load/Store
Store vector pair, immediate post-index, Q-form	STP	-	1/2	Load/Store
Store vector pair, immediate pre-index, S-form	STP	-	1	Load/Store
Store vector pair, immediate pre-index, D-form	STP	-	1	Load/Store
Store vector pair, immediate pre-index, Q-form	STP	-	1/2	Load/Store

3.16 ASIMD Integer data processing instructions

Table 3-15: AArch64 ASIMD Integer data processing instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD absolute diff	SABD, UABD	3	1	VALU
ASIMD absolute diff accum	SABA, UABA	6	2/5	VALU
ASIMD absolute diff accum long	SABAL2, UABAL2	6	2/5	VALU
ASIMD absolute diff long	SABDL2, UABDL2	3	1	VALU
ASIMD arith, basic	ABS, ADD, NEG, SHADD, SHSUB, SUB, UHADD, UHSUB	3	1	VALU
ASIMD arith, basic, long, saturate	SADDL, SADDL2, SADDW, SADDW2, SSUBL, SSUBL2, SSUBW, SSUBW2, UADDL, UADDL2, UADDW, UADDW2, USUBL, USUBL2, USUBW, USUBW2	3	1	VALU
ASIMD arith, complex	ADDHN, ADDHN2, SQABS, SQADD, SQNEG, SQSUB, SUBHN, SUBHN2, SUQADD, UQADD, UQSUB, USQADD	4	1	VALU
ASIMD arith, complex, rounding, add and subtract	RADDHN, RADDHN2, RSUBHN, RSUBHN2	8	2/5	VALU
ASIMD arith, complex, rounding halving addition	SRHADD, URHADD	3	1	VALU
ASIMD arith, pair-wise	ADDP, SADDLP, UADDLP	3	1	VALU
ASIMD arith, reduce, 4H/4S	ADDV, SADDLV, UADDLV	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD arith, reduce	ADDV	3	1	VALU
ASIMD arith, reduce Long	SADDLV, UADDLV	4	1	VALU
ASIMD compare	CMEQ, CMGE, CMGT, CMHI, CMHS, CMLE, CMLT	3	1	VALU
ASIMD compare test	CMTST	4	1	VALU
ASIMD dot product	SDOT, UDOT	4	1	VMAC
ASIMD dot product using signed and unsigned integers	SUDOT, USDOT	4	1	VMAC
ASIMD logical	AND, BIC, EOR, MOV, MVN, NOT, ORN, ORR	3	1	VALU
ASIMD matrix multiply-accumulate	SMMLA, UMMLA, USMMLA	4	1	VALU
ASIMD max/min, basic and pair-wise	SMAX, SMAXP, SMIN, SMINP, UMAX, UMAXP, UMIN, UMINP	3	1	VALU
ASIMD max/min, reduce, B-form	SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
ASIMD max/min, reduce, H-form	SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
ASIMD max/min, reduce, S-form	SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
ASIMD multiply	MUL, SQDMULH, SQRDMULH	4	1	VMAC
ASIMD multiply accumulate	MLA, MLS	4	1	VMAC
ASIMD multiply accumulate high	SQRDMLAH, SQRDMLSH	4	1	VMAC
ASIMD multiply accumulate long	SMLAL2, SMLSL2, UMLAL2, UMLSL2	4	1	VMAC
ASIMD multiply accumulate saturating long	SQDMLAL2, SQDMLSL2	4	1	VMAC
ASIMD multiply/multiply long (8x8) polynomial, D-form	PMUL, PMULL2	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD multiply/multiply long (8x8) polynomial, Q-form	PMUL, PMULL2	4	1	VALU
ASIMD multiply long	SMULL, SMULL2, UMULL, UMULL2, SQDMULL, SQDMULL2	4	1	VMAC
ASIMD pairwise add and accumulate long	SADALP, UADALP	7	2/5	VALU
ASIMD shift and accumulate	SRSRA, URSRA	7	2/5	VALU
ASIMD rounding shift and accumulate	SSRA, USRA	3	1	VALU
ASIMD shift by immediate, basic	SHL, SHLL2, SSHLL2, SSHR, SXTL2, USHLL2, USHR, UXTL2	3	1	VALU
ASIMD shift by immediate, narrow	SHRN2	4	1	VALU
ASIMD shift by immediate and insert, basic	SLI, SRI	3	1	VALU
ASIMD shift by immediate, complex	RSHRN2, SQRSHRN2, SQRSHRUN2, SQSHL, SQSHLU, SQSHRN2, SQSHRUN2, UQRSHRN2, UQSHL, UQSHRN2	4	1	VALU
ASIMD shift by register, basic	SSHL, USHL, SRSHL, SRSHR, URSHL, URSHR	3	1	VALU
ASIMD shift by register, complex	SQRSHL, SQSHL, UQRSHL, UQSHL	4	1	VALU

3.17 ASIMD Floating-point data processing instructions

Table 3-16: AArch64 ASIMD Floating-point data processing instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD FP absolute value/difference	FABS, FABD	4	1	VALU
ASIMD FP arith, normal	FADD, FSUB, FADDP	4	1	VALU
ASIMD FP compare	FACGE, FACGT, FCMEQ, FCMGE, FCMGT, FCMLE, FCMLT	3	1	VALU
ASIMD FP complex add	FCADD	4	1	VMAC
ASIMD FP complex multiply add	FCMLA	4	1	VMAC
ASIMD FP convert, long (F16 to F32)	FCVTL, FCVTL2	4	1	VALU
ASIMD FP convert, long (F32 to F64)	FCVTL, FCVTL2	4	1	VALU
ASIMD FP convert, narrow (F32 to F16)	FCVTN, FCVTN2	4	1	VALU
ASIMD FP convert, narrow (F64 to F32)	FCVTN, FCVTN2, FCVTXN2	4	1	VALU
ASIMD FP convert, from gen to vec reg	SCVTF, UCVTF	4	1	VALU
ASIMD FP convert, other, F16	FCVTAS, FCVTAU, FCVTMS, FCVTMU, FCVTNS, FCVTNU, FCVTPS, FCVTPU, FCVTZS, FCVTZU	4	1	VALU
ASIMD FP convert, other, F32	FCVTAS, FCVTAU, FCVTMS, FCVTMU, FCVTNS, FCVTNU, FCVTPS, FCVTPU, FCVTZS, FCVTZU	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD FP convert, other, F64	FCVTAS, FCVTAU, FCVTMS, FCVTMU, FCVTNS, FCVTNU, FCVTPS, FCVTPU, FCVTZS, FCVTZU	4	1	VALU
ASIMD FP divide, D-form, F16	FDIV	8	2/5	VMC
ASIMD FP divide, D-form, F32	FDIV	13	1/5	VMC
ASIMD FP divide, Q-form, F16	FDIV	8	1/5	VMC
ASIMD FP divide, Q-form, F32	FDIV	13	1/10	VMC
ASIMD FP divide, Q-form, F64	FDIV	22	1/19	VALU
ASIMD FP max/min, normal	FMAX, FMAXNM, FMIN, FMINNM	4	1	VALU
ASIMD FP max/min, pairwise	FMAXP, FMAXNMP, FMINP, FMINNMP	4	1	VALU
ASIMD FP max/min, reduce	FMAXV, FMAXNMV, FMINV, FMINNMV	4	1	VALU
ASIMD FP multiply	FMUL, FMULX	4	1	VMAC
ASIMD FP multiply accumulate	FMLA, FMLS	4	1	VMAC
ASIMD FP multiply accumulate long	FMLAL, FMLAL2, FMLSL, FMLSL2	4	1	VMAC
ASIMD FP negate	FNEG	4	1	VALU
ASIMD FP round, F16	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ, FRINT32X, FRINT64X, FRINT32Z, FRINT64Z	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD FP round, F32	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ, FRINT32X, FRINT64X, FRINT32Z, FRINT64Z	4	1	VALU
ASIMD FP round, F64	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ, FRINT32X, FRINT64X, FRINT32Z, FRINT64Z	4	1	VALU
ASIMD FP square root, D-form, F16	FSQRT	8	2/5	VMC
ASIMD FP square root, D-form, F32	FSQRT	12	2/9	VMC
ASIMD FP square root, Q-form, F16	FSQRT	8	1/5	VMC
ASIMD FP square root, Q-form, F32	FSQRT	12	1/9	VMC
ASIMD FP square root, Q-form, F64	FSQRT	22	1/19	VMC

**Note**

Floating-point division operations may finish early if the divisor is a power of two.

3.18 ASIMD BFloat16 (BF16) instructions

Table 3-17: AArch64 ASIMD BFloat16 (BF16) instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD convert, F32 to BF16	BFCVTN, BFCVTN2	4	1	VALU
ASIMD dot product	BFDOT	11	1	VMAC,VALU
ASIMD matrix multiply accumulate	BFMMLA	16	2/5	VMAC,VALU
ASIMD multiply accumulate long	BFMLALB, BFMLALT	4	1	VMAC
Scalar convert, F32 to BF16	BFCVT	4	1	VALU

3.19 ASIMD miscellaneous instructions

Table 3-18: AArch64 ASIMD miscellaneous instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD bit reverse	RBIT	3	1	VALU
ASIMD bitwise insert	BIF, BIT, BSL	3	1	VALU
ASIMD count	CLS, CLZ, CNT	3	1	VALU
ASIMD duplicate, gen reg	DUP	3	1	VALU
ASIMD duplicate, element	DUP	3	1	VALU
ASIMD extract	EXT	3	1	VALU
ASIMD extract narrow	XTN	4	1	VALU
ASIMD extract narrow, saturating	SQXTN, SQXTN2, SQXTUN, SQXTUN2, UQXTN, UQXTN2	4	1	VALU
ASIMD insert, element to element	INS	3	1	VALU
ASIMD move, FP immediate	MOV	3	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD FP convert, from vec to vec reg	FCVT, FCVTXN	4	1	VALU
ASIMD move, FP immediate	FMOV	3	1	VALU
ASIMD move, FP register	FMOV	3	2	VALU
ASIMD move, FP transfer, from gen to vec reg	FMOV	3	1	VALU
ASIMD move, integer immediate	MOVI, MVNI	3	1	VALU
ASIMD reciprocal estimate, F16	FRECPE, FRECPX, FRSQRTE, URECPE, URSQRTE	4	1	VMAC
ASIMD reciprocal estimate, F32	FRECPE, FRECPX, FRSQRTE, URECPE, URSQRTE	4	1	VMAC
ASIMD reciprocal estimate, F64	FRECPE, FRECPX, FRSQRTE, URECPE, URSQRTE	4	1	VMAC
ASIMD reciprocal step	FRECPS, FRSQRTS	4	1	VMAC
ASIMD reverse	REV16, REV32, REV64	3	1	VALU
ASIMD table lookup, 1 table regs	TBL	4	1	VALU
ASIMD table lookup, 2 table regs	TBL	8	2/5	VALU
ASIMD table lookup, 3 table regs	TBL	12	1/5	VALU
ASIMD table lookup, 4 table regs	TBL	16	1/9	VALU
ASIMD table lookup extension, 1 table reg	TBX	8	2/5	VALU
ASIMD table lookup extension, 2 table regs	TBX	12	1/5	VALU
ASIMD table lookup extension, 3 table regs	TBX	16	1/9	VALU
ASIMD table lookup extension, 4 table regs	TBX	20	1/13	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD transfer, element to gen reg	UMOV, SMOV	3	1	VALU
ASIMD transfer, gen reg to element	INS	3	1	VALU
ASIMD transpose	TRN1, TRN2	3	1	VALU
ASIMD unzip/zip	UZP1, UZP2, ZIP1, ZIP2	3	1	VALU

3.20 ASIMD load instructions

The latencies shown assume the memory access hits in the Level 1 Data Cache. Base register updates are done in parallel to the operation.

Table 3-19: AArch64 ASIMD load instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD load, 1 element, multiple, 1 reg, D-form	LD1	3	1	Load/Store
ASIMD load, 1 element, multiple, 1 reg, Q-form	LD1	3	1	Load/Store
ASIMD load, 1 element, multiple, 2 reg, D-form	LD1	3	1	Load/Store
ASIMD load, 1 element, multiple, 2 reg, Q-form	LD1	4	1/2	Load/Store
ASIMD load, 1 element, multiple, 3 reg, D-form	LD1	4	1/2	Load/Store
ASIMD load, 1 element, multiple, 3 reg, Q-form	LD1	5	1/3	Load/Store
ASIMD load, 1 element, multiple, 4 reg, D-form	LD1	4	1/2	Load/Store
ASIMD load, 1 element, multiple, 4 reg, Q-form	LD1	6	1/4	Load/Store
ASIMD load, 1 element, one lane, B/H/S	LD1	3	1	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD load, 1 element, one lane, D	LD1	3	1	Load/Store
ASIMD load, 1 element, all lanes, D-form	LD1R	3	1	Load/Store
ASIMD load, 1 element, all lanes, Q-form	LD1R	3	1	Load/Store
ASIMD load, 2 element, multiple, D-form	LD2	4	2/3	Load/Store
ASIMD load, 2 element, multiple, Q-form	LD2	4	3/7	Load/Store
ASIMD load, 2 element, one lane, B/H/S	LD2	4	1/6	Load/Store
ASIMD load, 2 element, one lane, D	LD2	4	1/6	Load/Store
ASIMD load, 2 element, all lanes, D-form	LD2R	3	1/2	Load/Store
ASIMD load, 2 element, all lanes, Q-form	LD2R	3	1/2	Load/Store
ASIMD load, 3 element, multiple, D-form	LD3	5	1/6	Load/Store
ASIMD load, 3 element, multiple, Q-form	LD3	5	1/6	Load/Store
ASIMD load, 3 element, one lane, B/H/S	LD3	5	1/7	Load/Store
ASIMD load, 3 element, one lane, D	LD3	5	1/7	Load/Store
ASIMD load, 3 element, all lanes, D-form	LD3R	4	1/3	Load/Store
ASIMD load, 3 element, all lanes, Q-form	LD3R	4	1/3	Load/Store
ASIMD load, 4 element, multiple, D-form	LD4	5	1/7	Load/Store
ASIMD load, 4 element, multiple, Q-form	LD4	5	1/8	Load/Store
ASIMD load, 4 element, one lane, B/H/S	LD4	6	1/7	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD load, 4 element, one lane, D	LD4	6	1/7	Load/Store
ASIMD load, 4 element, all lanes, D-form	LD4R	4	1/4	Load/Store
ASIMD load, 4 element, all lanes, Q-form	LD4R	4	1/4	Load/Store

3.21 ASIMD store instructions

Base register updates are done in parallel to the operation.

Table 3-20: AArch64 ASIMD store instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD store, 1 element, multiple, 1 reg, D-form	ST1	-	1	Load/Store
ASIMD store, 1 element, multiple, 1 reg, Q-form	ST1	-	1	Load/Store
ASIMD store, 1 element, multiple, 2 reg, D-form	ST1	-	1	Load/Store
ASIMD store, 1 element, multiple, 2 reg, Q-form	ST1	-	1/2	Load/Store
ASIMD store, 1 element, multiple, 3 reg, D-form	ST1	-	1/2 ^[4]	Load/Store
ASIMD store, 1 element, multiple, 3 reg, Q-form	ST1	-	1/3	Load/Store
ASIMD store, 1 element, multiple, 4 reg, D-form	ST1	-	1/2	Load/Store
ASIMD store, 1 element, multiple, 4 reg, Q-form	ST1	-	1/4	Load/Store
ASIMD store, 1 element, one lane, B/H/S	ST1	-	1	Load/Store
ASIMD store, 1 element, one lane, D	ST1	-	1	Load/Store

^[4] Throughput=1/3 when the access is aligned and crosses 16B boundary, one more cycle is needed.

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
ASIMD store, 2 element, multiple, D-form	ST2	-	1	Load/Store
ASIMD store, 2 element, multiple, Q-form	ST2	-	1/2	Load/Store
ASIMD store, 2 element, one lane, B/H/S	ST2	-	1	Load/Store
ASIMD store, 2 element, one lane, D	ST2	-	1	Load/Store
ASIMD store, 3 element, multiple, D-form, B/H/S	ST3	-	1/4	Load/Store
ASIMD store, 3 element, multiple, Q-form, B/H/S	ST3	-	1/6	Load/Store
ASIMD store, 3 element, multiple, Q-form, D	ST3	-	1/3	Load/Store
ASIMD store, 3 element, one lane, B/H/S	ST3	-	1/2	Load/Store
ASIMD store, 3 element, one lane, D	ST3	-	1/2	Load/Store
ASIMD store, 4 element, multiple, D-form, B/H/S	ST4	-	1/4	Load/Store
ASIMD store, 4 element, multiple, Q-form, B/H/S	ST4	-	1/8	Load/Store
ASIMD store, 4 element, multiple, Q-form, D	ST4	-	1/4	Load/Store
ASIMD store, 4 element, one lane, B/H/S	ST4	-	1/2	Load/Store
ASIMD store, 4 element, one lane, D	ST4	-	1/2	Load/Store

3.22 Cryptography extensions

Table 3-21: AArch64 Cryptography instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Crypto AES ops	AESD, AESE, AESIMC, AESMC	3	1	Crypto
Crypto polynomial (64x64) multiply long	PMULL, PMULL2	4	1	VMC
Crypto SHA1 hash acceleration op	SHA1H	3	1	VALU
Crypto SHA1 hash acceleration ops	SHA1C, SHA1M, SHA1P	4	1	VMC
Crypto SHA1 schedule acceleration ops	SHA1SU0, SHA1SU1	3	1	VMC
Crypto SHA256 hash acceleration ops	SHA256H, SHA256H2	4	1	VMC
Crypto SHA256 schedule acceleration ops	SHA256SU0, SHA256SU1	4	1	VMC
Crypto SHA512 hash acceleration ops	SHA512H, SHA512H2, SHA512SU0, SHA512SU1	9	1/9	VMC
Crypto SHA3 ops	BCAX, EOR3	3	1	VALU
Crypto SHA3 ops, exclusive Or and rotate	XAR	4	1	VALU
Crypto SHA3 ops, rotate and exclusive Or	RAX1	9	1/9	VMC
Crypto SM3 ops	SM3PARTW1, SM3PARTW2, SM3SS1, SM3TT1A, SM3TT1B, SM3TT2A, SM3TT2B	9	1/9	VMC
Crypto SM4 ops	SM4E, SM4EKEY	9	1/9	VMC

3.23 CRC

Table 3-22: AArch64 CRC instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
CRC checksum ops	CRC32, CRC32C, CRC32B, CRC32CB, CRC32CH, CRC32CW, CRC32CX, CRC32H, CRC32W, CRC32X	2	1	MAC

3.24 SVE Predicate instructions

Table 3-23: SVE Predicate instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Loop control, based on predicate	BRKA, BRKB	2	1	PALU
Loop control, based on predicate and flag setting	BRKAS, BRKBS	2	1	PALU
Loop control, propagating	BRKN, BRKPA, BRKPB	2	1	PALU
Loop control, propagating and flag setting	BRKNS, BRKPAS, BRKPBS	2	1	PALU
Loop control, based on GPR	WHILEGE, WHILEGT, WHILEHI, WHILEHS, WHILELE, WHILELO, WHILELS, WHILELT, WHILERW, WHILEWR	2	1	PALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Loop terminate	CTERMEQ, CTERMNE	1	1	ALU
Predicate counting scalar, add	ADDPL, ADDVL, RDVL	1	1	ALU
Predicate counting scalar	CNTB, CNTH, CNTW, CNTD, DECB, DECH, DECW, DECD, INCB, INCH, INCW, INCD	3	1	ALU
Predicate counting scalar, saturate	SQDECB, SQDECH, SQDECW, SQDECD, SQINCB, SQINCH, SQINCW, SQINCD, UQDECB, UQDECH, UQDECW, UQDECD, UQINCB, UQINCH, UQINCW, UQINCD	5	1	ALU
Predicate counting scalar, active predicate	CNTP, DECP, INCP	1	1	PALU
Predicate counting scalar, active predicate, saturating, 64-bit	SQDECP, SQINCP, UQDECP, UQINCP	9	2/7	VALU
Predicate counting scalar, active predicate, saturating, 32-bit	SQDECP, SQINCP	3	2/7	VALU
Predicate counting scalar, active predicate, saturating, 32-bit	UQDECP, UQINCP	9	2/7	VALU
Predicate counting vector, active predicate	CNTP, DECP, INCP	3	1	PALU
Predicate counting vector, active predicate, saturating	SQDECP, SQINCP, UQDECP, UQINCP	4	1	VALU
Predicate logical	AND, BIC, EOR, MOV, NAND, NOR, NOT, ORN, ORR	2	1	PALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Predicate logical, flag setting	ANDS, BICS, EORS, MOVS, NANDS, NORs, NOTS, ORNS, ORRS	2	1	PALU
Predicate reverse	REV	1	1	PALU
Predicate select	SEL	2	1	PALU
Predicate set	PFALSE, PTRUE	1	1	PALU
Predicate set/initialize, set flags	PTRUES	2	1	PALU
Predicate find first/next	PFIRST, PNEXT	2	1	PALU
Predicate test	PTEST	1	1	PALU
Predicate transpose	TRN1, TRN2	1	1	PALU
Predicate unpack and widen	PUNPKHI, PUNPKLO	1	1	PALU
Predicate zip/unzip	ZIP1, ZIP2, UZP1, UZP2	1	1	PALU

3.25 SVE Integer instructions

Table 3-24: SVE integer instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Arithmetic, absolute diff	SABD, UABD	3	1	VALU
Arithmetic, absolute diff accum	SABA, UABA	6	2/5	VALU
Arithmetic, absolute diff accum long	SABALB, SABALT, UABALB, UABALT	6	2/5	VALU
Arithmetic, absolute diff long	SABDLB, SABDLT, UABDLB, UABDLT	3	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Arithmetic, basic	ABS, ADD, ADR, CNOT, NEG, SHADD, SHSUB, SHSUBR, SRHADD, SUB, UADDWB, UADDWT, UHADD, UHSUB, UHSUBR, URHADD	3	1	VALU
Arithmetic, basic	SUBHNB, SUBHNT, SUBR, USUBWB, USUBWT	4	1	VALU
Arithmetic, basic	SADDLB, SADDLBT, SADDLT, SADDWB, SADDWT, SSUBLB, SSUBLBT, SSUBLT, SSUBLTB, SSUBWB, SSUBWT, UADDLB, UADDLT, USUBLB, USUBLT	4	1	VALU
Arithmetic, complex	ADDHNB, ADDHNT, SQABS, SQADD, SQNEG, SQSUB, QSUBR, SUQADD, UQADD, UQSUB, UQSUBR, USQADD	4	1	VALU
Arithmetic, complex	RADDHNB, RADDHNT, RSUBHNB, RSUBHNT	8	2/5	VALU
Arithmetic, large integer	ADCLB, ADCLT, SBCLB, SBCLT	4	1	VALU
Arithmetic, pairwise add	ADDP	3	1	VALU
Arithmetic, pairwise add and accum long	SADALP, UADALP	7	2/5	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Arithmetic, shift	ASR, ASRR, LSL, LSLR, LSR, LSRR	3	1	VALU
Arithmetic, shift and accumulate	USRA	4	1	VALU
Arithmetic, shift and accumulate complex, round	SRSRA, URSRA	7	2/5	VALU
Arithmetic, shift and accumulate complex	SSRA	4	1	VALU
Arithmetic, shift by immediate	SHRNB, SHRNT, SSHLLB, SSHLLT, USHLLB, USHLLT	3	1	VALU
Arithmetic, shift by immediate and insert	SLI, SRI	3	1	VALU
Arithmetic, shift complex	RSHRNB, RSHRNT, SQRSHL, SQRSHLR, SQRSHRNB, SQRSHRNT, SQRSHRUNB, SQRSHRUNT, SQSHL, SQSHLR, SQSHLU, SQSHRNB, SQSHRNT, SQSHRUNB, SQSHRUNT, UQRSHL, UQRSHLR, UQRSHRNB, UQRSHRNT, UQSHL, UQSHLR, UQSHRNB, UQSHRNT	4	1	VALU
Arithmetic, shift right for divide	ASRD	4	1	VALU
Arithmetic, shift rounding	SRSHL, SRSHLR, SRSHR, URSHL, URSHLR, URSHR	4	1	VALU
Bit manipulation (B)	BDEP, BEXT, BGRP	13	1/13	VMC

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Bit manipulation (H)	BDEP, BEXT, BGRP	21	1/21	VMC
Bit manipulation (S)	BDEP, BEXT, BGRP	37	1/37	VMC
Bit manipulation (D)	BDEP, BEXT, BGRP	68	1/68	VMC
Bitwise select	BSL, BSL1N, BSL2N, NBSL	3	1	VALU
Count/reverse bits	CLS, CLZ, RBIT	3	1	VALU
Count (B,H)	CNT	3	1	VALU
Count (S)	CNT	8	2/5	VALU
Count (D)	CNT	12	1/5	VALU
Broadcast logical bitmask immediate to vector	DUPM	4	1	VALU
Compare and set flags	CMPEQ, CMPGE, CMPGT, CMPHI, CMPHS, CMPLE, CMPLO, CMPLS, CMPLT, CMPNE	5	1	VALU
Complex add	CADD	3	1	VALU
Complex add saturating	SQCADD	4	1	VALU
Complex dot product 8-bit element	CDOT	4	1	VMAC
Complex dot product 16-bit element	CDOT	4	1	VMAC
Complex multiply-add B, H, S element size	CMLA	4	1	VMAC
Complex multiply-add D element size	CMLA	4	1	VMAC
Conditional extract operations, general purpose register	CLASTA, CLASTB	3	2/7	VALU
Conditional extract operations, SIMD&FP scalar and vector forms	CLASTA, CLASTB, COMPACT, SPLICE	4	1	VALU
Convert to floating point, 64b to float or convert to double	SCVTF, UCVTF	4	1	VALU
Convert to floating point, 32b to single or half	SCVTF, UCVTF	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Convert to floating point, 16b to half	SCVTF, UCVTF	4	1	VALU
Copy	CPY	3	1	VALU
Divides, 32 bit	SDIV, SDIVR, UDIV, UDIVR	15	1/12	VMC
Divides, 64 bit	SDIV, SDIVR, UDIV, UDIVR	26	1/23	VMC
Dot product, 8 bit	SDOT, UDOT	4	1	VMAC
Dot product, 8 bit, using signed and unsigned integers	SUDOT, USDOT	4	1	VMAC
Dot product, 16 bit	SDOT, UDOT	4	1	VMAC
Duplicate, immediate and indexed form	DUP	3	1	VALU
Duplicate, indexed > elem	DUP	3	1	VALU
Duplicate, scalar form	DUP	3	1	VALU
Extend, sign or zero	SXTB, SXTH, SXTW, UXTB, UXTH, UXTW	3	1	VALU
Extract	EXT	3	1	VALU
Extract narrow saturating	SQXTNB, SQXTNT, SQXTUNB, SQXTUNT, UQXTNB, UQXTNT, UQXTUNB, UQXTUNT	4	1	VALU
Extract/insert operation, SIMD and FP scalar form	LASTA, LASTB, INSR	4	1	VALU
Extract operation, scalar	LASTA, LASTB	8	2/7	VALU
Insert operation, scalar	INSR	4	1	VALU
Histogram operations	HISTCNT, HISTSEG	8	2/5	VALU
Horizontal operations, B, H, S form, immediate operands only	INDEX	4	1	VMAC

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Horizontal operations, B, H, S form, scalar, immediate operands or immediate, scalar operands	INDEX	4	1	VMAC
Horizontal operations, D form, immediate operands only	INDEX	4	1	VMAC
Horizontal operations, D form, scalar, immediate operands or immediate, scalar operands	INDEX	4	1	VMAC
Logical ops	AND, BIC, EON, EOR, MOV, NOT, ORN, ORR	3	1	VALU
Logical, exclusive or bottom-top and top-bottom	EORBT, EORTB	4	1	VALU
Max/min, basic and pairwise	SMAX, SMAXP, SMIN, SMINP, UMAX, UMAXP, UMIN, UMINP	3	1	VALU
Matching operations	MATCH, NMATCH	9	2/7	VALU
Matrix multiply-accumulate	SMMLA, UMMLA, USMMLA	4	1	VMAC
Move prefix	MOVPRFX	3	1	VALU
Multiply, B, H, S element size	MUL, SMULH, UMULH	4	1	VMAC
Multiply, D element size	MUL, SMULH, UMULH	4	1	VMAC
Multiply long	SMULLB, SMULLT, UMULLB, UMULLT	4	1	VMAC
Multiply accumulate, B, H, S element size	MLA, MLS, MAD, MSB	4	1	VMAC
Multiply accumulate, D element size	MLA, MLS, MAD, MSB	4	1	VMAC
Multiply accumulate long	SMLALB, SMLALT, SMLSLB, SMLSLT, UMLALB, UMLALT, UMLSLB, UMLSLT	4	1	VMAC

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Multiply accumulate saturating doubling long regular	SQDMLALB, SQDMLALT, SQDMLALBT, SQDMLSLB, SQDMLSLT, SQDMLSLBT	4	1	VMAC
Multiply saturating doubling high, B, H, S element size	SQDMULH	4	1	VMAC
Multiply saturating doubling high, D element size	SQDMULH	4	1	VMAC
Multiply saturating doubling long	SQDMULLB, SQDMULLT	4	1	VMAC
Multiply saturating rounding doubling regular/complex accumulate, B, H, S element size	SQRDMLAH, SQRDMLSH, SQRDCMLAH	4	1	VMAC
Multiply saturating rounding doubling regular/complex accumulate, D element size	SQRDMLAH, SQRDMLSH, SQRDCMLAH	4	1	VMAC
Multiply saturating rounding doubling regular/complex, B, H, S element size	SQRDMULH	4	1	VMAC
Multiply saturating rounding doubling regular/complex, D element size	SQRDMULH	4	1	VMAC
Multiply/multiply long, (8, 16, 32) polynomial	PMUL, PMULLB, PMULLT	4	1	VALU
Multiply/multiply long, (64) polynomial	PMULLB, PMULLT	9	1/9	VMC
Predicate counting vector	DECB, DECH, DECW, DECD, INCB, INCH, INCW, INCD	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Predicate counting vector, saturating	SQDECB, SQDECH, SQDECW, SQDECD, SQINCB, SQINCH, SQINCW, SQINCD, UQDECB, UQDECH, UQDECW, UQDECD, UQINCB, UQINCH, UQINCW, UQINCD	4	1	VALU
Reciprocal estimate	URECPE, URSQRTE	4	1	VMAC
Reduction, arithmetic, B form	SADDV, UADDV, SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
Reduction, arithmetic, H form	SADDV, UADDV, SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
Reduction, arithmetic, S form	SADDV, UADDV, SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
Reduction, arithmetic, D form	SADDV, UADDV, SMAXV, SMINV, UMAXV, UMINV	4	1	VALU
Reduction, logical	ANDV, EORV, ORV	4	1	VALU
Reverse, vector	REV, REVB, REVH, REVW	3	1	VALU
Select, vector form	SEL	3	1	VALU
Table lookup	TBL	4	1	VALU
Table lookup, double table	TBL	8	2/5	VALU
Table lookup extension	TBX	4	1	VALU
Transpose, vector form	TRN1, TRN2	3	1	VALU
Unpack and extend	SUNPKHI, SUNPKLO, UUNPKHI, UUNPKLO	4	1	VALU
Zip/unzip	UZP1, UZP2, ZIP1, ZIP2	3	1	VALU

3.26 SVE Floating-point data processing instructions

Table 3-25: SVE Floating-point data processing instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Floating point absolute value/difference	FABD, FABS	4	1	VALU
Floating point arithmetic	FADD, FADDP, FNEG, FSUB, FSUBR	4	1	VALU
Floating point associative add, F16	FADDA	25	1/25	VALU
Floating point associative add, F32	FADDA	9	1/9	VALU
Floating point associative add, F64	FADDA	3	2/5	VALU
Floating point compare	FACGE, FACGT, FACLE, FACLT, FCMEQ, FCMGE, FCMGT, FCMLE, FCMLT, FCMNE, FCMUO	5	1	VALU
Floating point complex add	FCADD	4	1	VALU
Floating point complex multiply add	FCMLA	4	1	VMAC
Floating point convert, long to narrow	FCVT, FCVTLT, FCVTNT	4	1	VALU
Floating point convert, round to odd	FCVTX, FCVTXNT	4	1	VALU
Floating point base2 log, F16	FLOGB	4	1	VMAC
Floating point base2 log, F32	FLOGB	4	1	VMAC
Floating point base2 log, F64	FLOGB	4	1	VMAC
Floating point convert to integer, F16	FCVTZS, FCVTZU	4	1	VALU
Floating point convert to integer, F32	FCVTZS, FCVTZU	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Floating point convert to integer, F64	FCVTZS, FCVTZU	4	1	VALU
Floating point copy	FCPY, FDUP, FMOV	3	1	VALU
Floating point divide, F16	FDIV, FDIVR	8	1/5	VMC
Floating point divide, F32	FDIV, FDIVR	13	1/10	VMC
Floating point divide, F64	FDIV, FDIVR	22	1/19	VMC
Floating point min/max pairwise	FMAXP, FMAXNMP, FMINP, FMINNMP	4	1	VALU
Floating point min/max	FMAX, FMIN, FMAXNM, FMINNM	4	1	VALU
Floating point multiply	FSCALE, FMUL, FMULX	4	1	VMAC
Floating point multiply accumulate	FMLA, FMLS, FMAD, FMSB, FNMAD, FNMLA, FNMLS, FNMSB	4	1	VMAC
Floating point multiply add/sub accumulate long	FMLALB, FMLALT, FMLSLB, FMLSLT	4	1	VMAC
Floating point reciprocal estimate, F16	FRECPE, FRECPX, FRSQRTE	4	1	VMAC
Floating point reciprocal estimate, F32	FRECPE, FRECPX, FRSQRTE	4	1	VMAC
Floating point reciprocal estimate, F64	FRECPE, FRECPX, FRSQRTE	4	1	VMAC
Floating point reciprocal step	FRECPS, FRSQRTS	4	1	VMAC
Floating point max/min reduction	FMAXNMV, FMAXV, FMINNMV, FMINV	4	1	VALU
Floating point reduction, F16	FADDV	12	1/5	VALU
Floating point reduction, F32	FADDV	8	2/5	VALU
Floating point reduction, F64	FADDV	4	1	VALU

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Floating point round to integral, F16	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ	4	1	VALU
Floating point round to integral, F32	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ	4	1	VALU
Floating point round to integral, F64	FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, FRINTZ	4	1	VALU
Floating point square root, F16	FSQRT	8	1/5	VMC
Floating point square root, F32	FSQRT	12	1/9	VMC
Floating point square root F64	FSQRT	22	1/19	VMC
Floating point trigonometric exponentiation	FEXPA	4	1	VMAC
Floating point trigonometric multiply add	FTMAD	4	1	VMAC
Floating point trigonometric starting value	FTSMUL	4	1	VMAC
Floating point trigonometric select coefficient	FTSSEL	3	1	VALU



Floating-point division operations may finish early if the divisor is a power of two.

3.27 SVE BFloat16 (BF16) instructions

Table 3-26: SVE Bfloat16 (BF16) instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Convert, F32 to BF16	BFCVT, BFCVTNT	4	1	VALU
Dot product	BFDOT	11	1	VMAC,VALU
Matrix multiply accumulate	BFMMLA	16	2/5	VMAC,VALU
Multiply accumulate long	BFMLALB, BFMLALT	4	1	VMAC

3.28 SVE Load instructions

The latencies shown in Table 3-27 assume the memory access hits in the Level 1 Data Cache. Base register updates are done in parallel to the operation.

Table 3-27: SVE Load instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Load vector	LDR	3	1	Load/Store
Load predicate	LDR	3	1	Load/Store
Contiguous load, scalar + imm	LD1B, LD1D, LD1H, LD1W, LD1SB, LD1SH, LD1SW	3	1	Load/Store
Contiguous load, scalar + scalar	LD1B, LD1D, LD1H, LD1W, LD1SB, LD1SH, LD1SW	3	1	Load/Store
Contiguous load broadcast, scalar + imm	LD1RB, LD1RH, LD1RD, LD1RW, LD1RSB, LD1RSH, LD1RSW, LD1RQB, LD1RQD, LD1RQH, LD1RQW	3	1	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Contiguous load broadcast, scalar + scalar	LD1RQB, LD1RQD, LD1RQH, LD1RQW	3	1	Load/Store
Non-temporal load, scalar + imm	LDNT1B, LDNT1D, LDNT1H, LDNT1W	3	1	Load/Store
Non-temporal load, scalar + scalar	LDNT1B, LDNT1D, LDNT1H, LDNT1W	3	1	Load/Store
Non-temporal gather load, vector + scalar 32-bit element size	LDNT1B, LDNT1H, LDNT1W, LDNT1SB, LDNT1SH	9	1/7	Load/Store
Non-temporal gather load, vector + scalar 64-bit element size	LDNT1B, LDNT1D, LDNT1H, LDNT1W, LDNT1SB, LDNT1SH, LDNT1SW	7	1/7	Load/Store
Contiguous first faulting load, scalar + scalar	LDFF1B, LDFF1D, LDFF1H, LDFF1W, LDFF1SB, LDFF1SD, LDFF1SH, LDFF1SW	3	1	Load/Store
Contiguous non-faulting load, scalar + imm	LDNF1B, LDNF1D, LDNF1H, LDNF1W, LDNF1SB, LDNF1SH, LDNF1SW	3	1	Load/Store
Contiguous load two structures to two vectors, scalar + imm	LD2B, LD2D, LD2H, LD2W	3	3/7	Load/Store
Contiguous load two structures to two vectors, scalar + scalar	LD2B, LD2D, LD2H, LD2W	3	3/7	Load/Store
Contiguous load three structures to three vectors, scalar + imm	LD3B, LD3D, LD3H, LD3W	5	1/6	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Contiguous load three structures to three vectors, scalar + scalar	LD3B, LD3D, LD3H, LD3W	5	1/6	Load/Store
Contiguous load four structures to four vectors, scalar + imm	LD4B, LD4D, LD4H, LD4W	5	1/8	Load/Store
Contiguous load four structures to four vectors, scalar + scalar	LD4B, LD4D, LD4H, LD4W	5	1/8	Load/Store
Gather load, vector + imm, 32-bit element size	LD1B, LD1H, LD1W, LD1SB, LD1SH, LD1SW, LDFF1B, LDFF1H, LDFF1W, LDFF1SB, LDFF1SH, LDFF1SW	9	1/7	Load/Store
Gather load, vector + imm, 64-bit element size	LD1B, LD1D, LD1H, LD1W, LD1SB, LD1SH, LD1SW, LDFF1B, LDFF1D, LDFF1H, LDFF1W, LDFF1SB, LDFF1SD, LDFF1SH, LDFF1SW	7	1/7	Load/Store
Gather load, 32-bit scaled offset	LD1H, LD1SH, LDFF1H, LDFF1SH, LD1W, LDFF1W, LDFF1SW	7	1/7	Load/Store
Gather load, 32-bit unpacked unscaled offset	LD1B, LD1SB, LDFF1B, LDFF1SB, LD1D, LDFF1D, LD1H, LD1SH, LDFF1H, LDFF1SH, LD1W, LD1SW, LDFF1W, LDFF1SW	7	1/7	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Gather load, 32-bit unscaled offset	LD1B, LD1H, LD1W, LDFF1B, LDFF1H, LDFF1SB, LDFF1SH, LDFF1W	7	1/7	Load/Store
Gather load, 32-bit unpacked scaled offset	LD1B, LD1SB, LDFF1B, LDFF1SB, LD1D, LDFF1D, LD1H, LD1SH, LDFF1H, LDFF1SH, LD1W, LD1SW, LDFF1W, LDFF1SW	7	1/7	Load/Store
Gather load, 64-bit unscaled offset	LD1B, LD1D, LD1H, LD1SB, LD1SH, LD1SW, LD1W, LDFF1B, LDFF1D, LDFF1H, LDFF1SB, LDFF1SH, LDFF1SW, LDFF1W	7	1/7	Load/Store
Gather load, 64-bit scaled offset	LD1B, LD1D, LD1H, LD1SB, LD1SH, LD1SW, LD1W, LDFF1B, LDFF1D, LDFF1H, LDFF1SB, LDFF1SH, LDFF1SW, LDFF1W	7	1/7	Load/Store

3.29 SVE Store instructions

Base register updates are done in parallel to the operation.

Table 3-28: SVE Store instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Store from predicate reg	STR	-	1	Load/Store
Store from vector reg	STR	-	1	Load/Store
Contiguous store, scalar + imm	ST1B, ST1H, ST1D, ST1W	-	1	Load/Store
Contiguous store, scalar + scalar	ST1H, ST1B, ST1D, ST1W	-	1	Load/Store
Contiguous store two structures from two vectors, scalar + imm	ST2B, ST2H, ST2D, ST2W	-	1/2	Load/Store
Contiguous store two structures from two vectors, scalar + scalar	ST2H, ST2B, ST2D, ST2W	-	1/2	Load/Store
Contiguous store three structures from three vectors, scalar + imm	ST3B, ST3H, ST3W	-	1/6	Load/Store
Contiguous store three structures from three vectors, scalar + imm, doubleword	ST3D	-	1/3	Load/Store
Contiguous store three structures from three vectors, scalar + scalar	ST3B, ST3H, ST3W	-	1/6	Load/Store
Contiguous store three structures from three vectors, scalar + scalar, doubleword	ST3D	-	1/3	Load/Store
Contiguous store four structures from four vectors, scalar + imm	ST4B, ST4H, ST4W	-	1/8	Load/Store
Contiguous store four structures from four vectors, scalar + imm, doubleword	ST4D	-	1/4	Load/Store

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Contiguous store four structures from four vectors, scalar + scalar	ST4B, ST4H, ST4W	-	1/8	Load/Store
Contiguous store four structures from four vectors, scalar + scalar, doubleword	ST4D	-	1/4	Load/Store
Non-temporal store, scalar + imm	STNT1B, STNT1D, STNT1H, STNT1W	-	4/5	Load/Store
Non-temporal store, scalar + scalar	STNT1H, STNT1B, STNT1D, STNT1W	-	4/5	Load/Store
Scatter non-temporal store, vector + scalar 32-bit element size	STNT1B, STNT1H, STNT1W	-	1/9	Load/Store
Scatter non-temporal store, vector + scalar 64-bit element size	STNT1B, STNT1D, STNT1H, STNT1W	-	1/8	Load/Store
Scatter store vector + imm 32-bit element size	ST1B, ST1H, ST1W	-	1/9	Load/Store
Scatter store vector + imm 64-bit element size	ST1B, ST1D, ST1H, ST1W	-	1/8	Load/Store
Scatter store, 32-bit scaled offset	ST1H, ST1W	-	1/9	Load/Store
Scatter store, 32-bit unpacked unscaled offset	ST1B, ST1D, ST1H, ST1W	-	1/8	Load/Store
Scatter store, 32-bit unpacked scaled offset	ST1D, ST1H, ST1W	-	1/8	Load/Store
Scatter store, 32-bit unscaled offset	ST1B, ST1H, ST1W	-	1/9	Load/Store
Scatter store, 64-bit unscaled offset	ST1B, ST1D, ST1H, ST1W	-	1/8	Load/Store
Scatter store, 64-bit scaled offset	ST1D, ST1H, ST1W	-	1/8	Load/Store

3.30 SVE Miscellaneous instructions

Table 3-29: SVE Miscellaneous instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Read first fault register, unpredicated	RDFFR	1	1	Load/Store
Read first fault register, predicated	RDFFR	3	1	Load/Store
Read first fault register and set flags	RDFFRS	3	1	Load/Store
Set first fault register	SETFFR	1	1	Load/Store
Write to first fault register	WRFFR	1	1	Load/Store

3.31 SVE Cryptography instructions

Table 3-30: SVE cryptography instructions

Instruction Group	AArch64 Instruction	Execution Latency	Execution Throughput	Utilized Pipeline
Crypto AES ops	AESD, AESE, AESIMC, AESMC	3	1	Crypto
Crypto SHA3 ops	BCAX, EOR3	3	1	VALU
Crypto SHA3 ops, exclusive Or and rotate	XAR	4	1	VALU
Crypto SHA3 ops RAX1	RAX1	9	1/9	VALU
Crypto SM4 ops	SM4E, SM4EKEY	9	1/9	VMC

4 Special considerations

4.1 Issue constraints

Cortex®-A320 Core is primarily a single issue CPU. However Cortex®-A320 Core is capable of dual-issuing a pair of instructions if the younger instruction is a direct branch instruction, or if the pair of instructions is a fused-pair (see 4.2 Instruction fusion.)

4.2 Instruction fusion

Cortex®-A320 Core can accelerate key instruction pairs in an operation called fusion.

The following instruction pairs can be fused for increased execution efficiency:

- 'AESE + AESMC' and 'AESD + AESIMC' (see 4.13)
- MOVPRFX fusion: Cortex®-A320 Core implements instruction fusion for MOVPRFX instructions followed by SVE data processing instructions in all cases where the instruction pair is defined as architecturally predictable other than those listed below, and the fused pair will execute with the latency of the SVE data processing instruction.
Due to microarchitectural limitations, the following instructions will not fuse with an unpredicated MOVPRFX: FCMLA, FMAD, FMLA, FMLS, FNMAD, FNMLA, FNMLS, FNMSB, MAD, MLA, MLS, MSB, UDOT, BFMLALB, BFMLALT, SMMLA, UMMLA, USMMLA, USDOT, SUDOT.
The following instructions will not fuse with a predicated or unpredicated MOVPRFX: CNT, SABA, SABALB, SABALT, UABA, UABALB, UABALT, URSRA.

4.3 Branch instruction alignment

Branch instruction density can affect performance.



For best case performance, avoid placing more than one conditional branch instructions within an aligned 16-byte instruction memory region.

4.4 Load / Store Alignment

The Armv8-A architecture allows many types of load and store accesses to be arbitrarily aligned. Cortex®-A320 Core handles most unaligned accesses without performance penalties. However, there are cases which could reduce bandwidth or incur additional latency, as described below.

- Quad-word load operations that are not 4-byte aligned.
- Load operations that cross a 32-byte boundary.
- Store operations that cross a 16-byte boundary.

4.5 A64 low latency pointer forwarding

In the A64 instruction set the following pointer sequence is expected to be common to generate load-store addresses:

```
adrp x0, <const>
ldrp x0, [x0, #1012 <const>]
```

In Cortex®-A320 Core, there are dedicated forwarding paths that always allow this sequence to be executed without incurring a dependency-based stall.

4.6 AUT* RET forwarding

In the A64 instruction set any variant of the AUT instruction will be dual issued with the directly following RET instruction. The latency of the AUT instruction for the dependency of the LR does not apply for these cases.

4.7 SIMD MAC forwarding

For the following integer SIMD instructions:

MUL, MLA, MLS, UMULL, UMULL2, SMULL, SMULL2, UMLAL, UMLAL2, SMLAL, SMLAL2, UMLSL, UMLSL2, SMLSL, SMLAL2, UDOT, SDOT

A dedicated MAC accumulator forwarding path is present. This forwarding path will be triggered only when two consecutive instructions satisfy the following conditions:

- Both instructions read from/write to the same destination/accumulator register.
- Both instructions use the same destination element size.
- The instructions target the same destination register size (128-bit or 64-bit).

When this forwarding path is active, the latency between the above instructions will be 1 cycle.

4.8 Memory Tagging Extensions

Enabling precise tag checking can prevent Cortex®-A320 Core from entering write-streaming mode. This can reduce performance and increase power for larger writes, and memset or memcpy-like workloads.

4.9 Memory routines

To achieve maximum throughput for memory copy (or similar loops), one should do the following:

- Unroll the loop to include multiple load and store operations per iteration, minimizing the overheads of looping.
- Stores should be aligned on a 16-byte boundary wherever possible.
- Loads should not cross a 32-byte boundary as they incur a penalty.



Note

Updated optimized routines are available:

<https://github.com/ARM-software/optimized-routines/tree/master/string/aarch64>

Figure 4-1 shows a code snippet from the inner loop of memory copy routine that copies at least 128 bytes. The loop copies 64 bytes per iteration and prefetches one iteration ahead.

Figure 4-1: Code Snippet from memcpy routine - large copy inner loop.

```
L(loop64_simd):
    str  A_q, [dst, 16]
    ldr  A_q, [src, 16]
    str  B_q, [dst, 32]
    ldr  B_q, [src, 32]
    str  C_q, [dst, 48]
    ldr  C_q, [src, 48]
    str  D_q, [dst, 64]!
    ldr  D_q, [src, 64]!
    subs count, count, 64
    b.hi L(loop64_simd)
```

Figure 4-2 shows a code snippet from the inner loop memory copy routine that copies 0 to 16 bytes.

Figure 4-2: Code Snippet from memcpy routine - small copy inner loop.

```

.p2align 4
/* Small copies: 0..16 bytes. */
L(copy16_simd):
/* 8-15 bytes. */
cmp    count, 8
b.lo   1f
ldr    A_l, [src]
ldr    A_h, [srcend, -8]
str    A_l, [dstin]
str    A_h, [dstend, -8]
ret
.p2align 4
1:
/* 4-7 bytes. */
tbz    count, 2, 1f
ldr    A_lw, [src]
ldr    A_hw, [srcend, -4]
str    A_lw, [dstin]
str    A_hw, [dstend, -4]
ret
---
bic    src, src, 15

```

To achieve maximum throughput on memset, it is recommended that one do the following.

Unroll the loop to include multiple store operations per iteration, minimizing the overheads of looping. Figure 4-3 shows code from the memset routine to set 17 to 96 bytes.

Figure 4-3: Code snippet from memset routine.

```

L(set_medium):
str    q0, [dstin]
tbnz   count, 6, L(set96)
str    q0, [dstend, -16]
tbz    count, 5, 1f
str    q0, [dstin, 16]
str    q0, [dstend, -32]
1:    ret

```

To achieve maximum performance on memset to zero, it is recommended that one use DC ZVA instead of STP. Figure 4-4 shows code from the memset routine to illustrate the usage of DC ZVA.

Figure 4-4: Code snippet from memset to zero routine.

```
L(zva_loop):  
    add dst, dst, 64  
    dc zva, dst  
    subs count, count, 64  
    b.hi L(zva_loop)  
    stp q0, q0, [dstend, -64]  
    stp q0, q0, [dstend, -32]  
    ret
```

4.10 Cache maintenance operations

While using set way invalidation operations on L1 cache, it is recommended that software be written to traverse the sets in the inner loop and ways in the outer loop.

4.11 Cache access latencies

The latency numbers for load instructions given in Instruction characteristics section assume the ideal case. It should be noted that more cycles will be added to these access delays depending on which level of cache is accessed. Table 4-1 lists the latencies for the different levels of cache.

Table 4-1: Cortex®-A320 cache access latencies

Scenario	Cycle count
L1 cache hit	4 cycles
L2 cache hit	10-12 cycles (10 is best case, 11-12 is normal case)

4.12 Shared VPU

Cortex®-A320 Core shares a VPU between up to two Cortex®-A320 cores in a complex. The VPU is used to execute ASIMD, FP, Neon, and SVE instructions. Instructions being executed on VPU pipelines by one core may reduce performance of the instructions executed on the VPU by the other core.

4.13 AES encryption / decryption

Cortex®-A320 Core implements instruction fusion for AES instructions (see section 4.2). It is recommended instructions pairs be interleaved in groups of three or more for the following: AESE, AESMC, AESD, AESIMC.

Figure 4-5: Code snippet for AES instruction fusion.

```
AESE  data0, key_reg
AESMC data0, data0
AESE  data1, key_reg
AESMC data1, data1
AESE  data2, key_reg
AESMC data2, data2...
```


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Revision history

These sections can help you understand how the document has changed over time.

Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

Document history

Issue	Date	Confidentiality	Change
01	26th February 2025	Non-Confidential	First release for launch.

Change history

The first table is for the first release. Then, each table compares the new issue of the manual with the last released issue of the manual. Issue numbers match the revision history in Release Information.

Table 4-3: Issue 01

Change	Location
First release for launch.	-